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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,256	01/24/2002	Edmund D. Blackshear	FIS9-2000-0273US1	7830

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FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

[REDACTED] EXAMINER

THAI, LUAN C

[REDACTED] ART UNIT [REDACTED] PAPER NUMBER

2827

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/056,256	BLACKSHEAR ET AL 
	Examiner Luan Thai	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 September 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 15-20 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-14 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 24 January 2002 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-14, in Paper No. 5, is acknowledged.

Information Disclosure Statement

2. The information disclosure statements (IDS) filed on 01/21/02 have been considered by the examiner.

Oath/Declaration

3. The declaration filed 01/24/02 is acceptable.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 5-8, 10, and 12-14, are rejected under 35 U.S.C. 102(b) as being anticipated by Miremadi et al (5,854,507).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 3, 5, 6, 8, 10, 12, and 13, Miremadi et al. disclose (see specifically figures 1-3 and 8) a memory structure comprising: a plurality of substrates 51-57 stacked one on another and connecting to one another via a plurality of connectors (or solder balls) 19; plurality of memory chip packages 63/25 and 65/25 mounted on

substrates 57 and 51 respectively, wherein the connectors (or solder balls) 19 have a size sufficient to form a gap between the substrates 51-57, and wherein the gap is larger than a height of the memory chip packages 63/25 and 65/25. Miremadi et al. further disclose a thermal connection 38 disposed between a top of the memory chip package 25/63 and a bottom of an adjacent substrate 51, such that the thermal connection 38 fills the gap. Miremadi et al. also disclose memory chip packages 63/25 and 65/25 including single memory chips 63 and 65 respectively, wherein the memory chip package and the substrates include identical electrical connections (or solder balls).

Regarding claims 7 and 14, although Miremadi et al. do not explicitly disclose the memory chip having an array of memory elements, this feature is taken to be inherent in Miremadi et al.'s device since the memory chips 63-65 of Miremadi et al's device are DRAM ICs (Col. 4, lines 4+), which appear to contain an array of memory elements.

6. Claims 1-4, 7-11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Moresco et al. (5,655,290).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 3, 4, 8, 10, and 11, Moresco et al. disclose (see specifically figure 1) a memory structure comprising: a plurality of substrates 100a-100c stacked one on another and connecting to one another via a plurality of connectors 150; plurality of memory chip packages 110/140 mounted on each of substrates 100a-100c, wherein the connectors 150 have a size sufficient to form a gap between the substrates 100a-100c, and wherein the gap is larger than a height of the memory chip packages 110/140.

Moresco et al. further disclose the memory chip packages and the substrates including identical electrical connections, and each of memory chip packages 110/140 including a single memory chip 110.

Regarding claims 2 and 9, Moresco et al. further disclose the memory chip package being tested before being mounted on the substrates (Col. 4, lines 1+).

Regarding claims 7 and 14, although Moresco et al. do not explicitly disclose the memory chip 110 having an array of memory elements, this feature is taken to be inherent in Moresco et al.'s device since a memory chip appears to contain an array of memory elements.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Luan Thai
November 23, 2002